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| EXAMINER | |
|---|---|
| DSOUZA, JOSEPH FRANCIS A | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/615,100 | TRAEBER, MARIO | |
| | Examiner | Art Unit | |
| | Adolf DSouza | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 - 8, 10-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8, 10-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

### *Response to Arguments*

1. Examiner has accepted changes Applicant has made to the Abstract, Specification and Claims in response to the objections made in the last Office Action (9/7/2006), except for the objection to the Arrangement of the Specification, which is repeated below.

2. Claim 9 (now cancelled) was objected to as being allowable in the last Office Action (9/7/2006). However, Examiner has found a new reference Shin (US 5,991,341) that is now being used to reject the limitations from claim 9 that were incorporated into independent claims 1 and 16.

### *Priority*

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

### *Specification*

4. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

**Arrangement of the Specification**

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 7, 10 – 13, 14 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsui et al.** (Low Power ACS Unit Design for the Viterbi Decoder; May 30, 1999; IEEE International Symposium on Circuits and Systems; pages 137 – 140; which has been provided by the Applicant in his Information Disclosure Statement) in

view of **Nguyen** (US 5,341,387) and further in view of **Chennakeshu et al.** (US 5,371,471) and **Shin** (US 5,991,341).

Regarding claim 1, Tsui discloses a Viterbi decoder for decoding a received sequence of data symbols which are coded using a predetermined coding instruction, and are transmitted via a transmission channel (page 1-137, section 2, 1st 7 lines), having:

(a) a branch metric calculation circuit for calculation of branch metrics for the received sequence of coded data symbols (Fig. 1, element BMU; page 1-137, section 2, paragraph starting with "1. Branch Metric unit (BMU) ...");

(b) a path metric calculation circuit for calculation of path metrics and decision values as a function of the branch metrics and the coding instruction, with the calculated path metrics (Fig. 1, element ACSU; page 1-137, section 2, paragraph starting with "2. Add-compare-select-unit (ACSU) ...")

Tsui does not disclose comparison with an adjustable threshold and storing those path metrics selected by comparing with the threshold and OR-ing the validity values from the path metric circuit.

In the same field of endeavor, however, Nguyen discloses comparing the path metric with an adjustable decision threshold value in order to produce an associated logic validity value, in which case the decision threshold value for the path metric

normalization can be set such that it is variable (column 4, lines 31 – 45; Fig. 11, elements 100, 102, 120; column 15, lines 21 - 39);

(c) a selection circuit which temporarily stores only those path metrics whose validity value is logic high in a memory, and selects from the temporarily stored path metrics that path with the optimum path metric, (Fig. 11,element 130, 134; column 4, lines 41 – 45).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Nguyen, in the system of Tsui because this would select only those path metrics that satisfied the threshold requirements, thereby reducing the computational and storage complexity.

In the same field of endeavor, however, Chennakeshu discloses using an increasing number of decision values being stored in the selection circuit as the signal-to-noise ratio of the transmission channel decreases (column 15, line 58 – column 16, line 28).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Chennakeshu, in the system of Tsui because this would improve the reliability of the decisions, as disclosed by Chennakeshu.

In the same field of endeavor, however, Shin discloses two or more logic validity values which are produced by the path metric calculation circuit are logically OR-linked by a logic circuit (Fig. 16, elements 434; column 16, lines 33 – 47; wherein the logic validity

values are interpreted as the MSBs of the path metrics new_pmo ...new_pm7) when the result of the logical OR linking is logic high (Fig. 16, element 438.1 – 438.8). (Nguyen above discloses the limitation regarding storing the values in the section circuit).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Shin, in the system of Tsui because normalization would prevent overflow, as disclosed by Shin (column 13, line 64 – column 14, line 5).

Regarding claim 2, Tsui discloses the selection circuit emits the data symbol sequence which is associated with the selected path for further data processing (Fig. 1, element SMU; page 1-137, right column, last 3 lines; wherein emitting the data symbol sequence is interpreted as outputting the decoded sequence u).

Regarding claim 3, Tsui does not disclose that comparator sets a logic value.

In the same field of endeavor, however, Nguyen discloses the path metric calculation circuit sets the validity value of logic high when the associated calculated path metric is less than the threshold value (column 4, lines 31 – 45; Fig. 11, output of element 120; column 15, lines 21 – 39).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Nguyen, in the system of Tsui because this would select only those path metrics that satisfied the threshold requirements, thereby reducing the computational and storage complexity.

Regarding claim 4, Tsui discloses that the selection circuit selects the path with the lowest calculated path metric (page 1-137, section 2, 1st paragraph, lines 3 - 7).

Regarding claim 5, Tsui discloses that the path metric calculation circuit contains two or more path metric calculation elements (Fig. 2, element 1 = upper adder/comp/adder and element 2 = lower adder/comp/adder combinations).

Regarding claim 6, Tsui discloses that a path metric calculation element in each case calculates the path metrics of two paths and compares them with one another, and emits the lower of the two path metrics to an associated clock memory element for temporary storage (Fig. 1 element ACSU and PMM; page 1-13, paragraph starting with "2. Add-compare-select-unit (ACSU):"; wherein the temporary storage is the path metric memory PMM).

Regarding claim 7, Tsui discloses Tsui discloses the path metric calculation element has: a first adder, which adds the branch metric of a first path and the metric of the first path which is temporarily stored in the associated clock memory element, and emits this to a first input of a multiplexer (Fig. 2, topmost adder; page 1-138, right column, paragraph starting with "Figure 2 shows.." – end of page);

a second adder, which adds the branch metric of a second path and the path metric of the second path which is temporarily stored in the associated clock memory element, and emits this to a second input of the multiplexer (Fig. 2, 2nd adder from top; page 1-138, right column, paragraph starting with "Figure 2 shows.." – end of page);

a first comparator circuit, which compares the sum values calculated by the two adders, with the comparison result being emitted as a decision value to the selection circuit and to the multiplexer as a control signal, with the multiplexer passing on the lower of the sum values calculated by the two adders to the associated clock register (Fig. 2, upper comparator; page 1-138, right column, paragraph starting with "Figure 2 shows.." – end of page).

All other limitations of claim 7 are as analyzed in claim 1 above (see what Nguyen discloses).

Regarding claim 10, Tsui discloses the path metrics are calculated sequentially by the path metric calculation elements (page 1-138, section 2.1; wherein one path metric calculation element is the adder/comp/adder set and the sequential computation is interpreted as the recursive computation).

Regarding claim 11, Tsui discloses that the number of path metrics, which correspond to the number N.sub.TS of states in a Trellis diagram, are calculated using 2.sup.K path metric calculation elements, and in that the number 2.sup.K of calculation element is

given by: 1 <= 2.sup.K <= (N.sub.TS)/2 (Fig. 2, wherein two elements are shown that is less than N.sub.TS/2).

Regarding claim 12, Tsui discloses that the path metric calculation elements are butterfly calculation elements, and in that the number 2.sup.K of calculation element is given by: 1 <= 2.sup.K <= (N.sub.TS)/2 (page 1-138, right column, paragraph starting with "Figure 2 shows ..", 1st 2 lines).

All other limitations of claim 12 are as analyzed as in claim 11 above.

Regarding claim 13, Tsui discloses that the path metric calculation elements are add-compare calculation elements, and in that the number 2.sup.K of calculation element is given by: 1 <= 2.sup.K <= (N.sub.TS) (Fig. 2, elements Adder and Comp; wherein the number of calculation elements is 3 per metric calculation element which is less than N.sub.TS).

Regarding claim 14, Tsui discloses the coding instruction is a Trellis code, which has 2.sup.L state transitions, where 0 <= L < infinity and L is a natural number (page 1-138, left column, section 2.1, lines 4 – 8; page 1-138, right column, paragraph starting with "Here BM(s,s0)...", 1st 2 lines; wherein the number of state transition is 2)

Regarding claim 15, Tsui discloses that the Trellis code has two state transitions (page 1-138, left column, section 2.1, lines 4 – 8; page 1-138, right column, paragraph starting with "Here BM(s,s0)...", 1st 2 lines).

Claims 16 is directed to method/steps of the same subject matter claimed in the apparatus claims 1- 2 and therefore, is rejected as explained in the rejections of claims 1-2 above.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsui et al.** (Low Power ACS Unit Design for the Viterbi Decoder; May 30, 1999; IEEE International Symposium on Circuits and Systems; pages 137 – 140; which has been provided by the Applicant in his Information Disclosure Statement) in view of **Nguyen** (US 5,341,387) and further in view of **Shin** (US 5,991,341), **Chennakeshu et al.** (US 5,371,471) and **Salembier et al.** (US 4,879,729).

Regarding claim 8, Tsui does not disclose that a threshold that is a power to two.

In the same field of endeavor, however, Nguyen discloses an adjustable decision threshold value (column 4, lines 31 – 45; Fig. 11, elements 100, 102, 120; column 15, lines 21 - 39).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Nguyen, in the system of Tsui because this would select only those path metrics that satisfied the threshold requirements, thereby reducing the computational and storage complexity.

Salembier discloses that a power value to the base two (column 4, lines 62 - 65).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Salembier, in the system of Tsui because this would result in reduced hardware complexity.

***Other Prior Art Cited***

The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to Viterbi decoders:

Reiner et al. (US 5,151,904) discloses use reconfigurable, multi-user Viterbi decoder.

Fredrickson et al. (US 5,327,440) discloses Viterbi trellis coding methods and apparatus for a direct access storage device.

Zehavi (US 5,469,452) discloses a Viterbi decoder bit efficient chain back memory method and decoder incorporating same.

Cesari et al. (US 5,912,908) discloses a Method of efficient branch metric computation for a Viterbi convolutional decoder.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolf DSouza whose telephone number is 571-272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
Examiner
Art Unit 2611

AD

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SUPERVISORY PATENT EXAMINER